

# OPT101 Monolithic Photodiode and Single-Supply Transimpedance Amplifier

## 1 Features

- Single Supply: 2.7 to 36 V
- Photodiode Size: 0.090 inch × 0.090 inch (2.29 mm × 2.29 mm)
- Internal 1-MΩ Feedback Resistor
- High Responsivity: 0.45 A/W (650 nm)
- Bandwidth: 14 kHz at  $R_F = 1\text{ M}\Omega$
- Low Quiescent Current: 120  $\mu\text{A}$
- Packages: Clear Plastic 8-pin PDIP and J-Lead SOP

## 2 Applications

- Medical Instrumentation
- Laboratory Instrumentation
- Position and Proximity Sensors
- Photographic Analyzers
- Barcode Scanners
- Smoke Detectors
- Currency Changers

## 3 Description

The OPT101 is a monolithic photodiode with on-chip transimpedance amplifier. The integrated combination of photodiode and transimpedance amplifier on a single chip eliminates the problems commonly encountered in discrete designs, such as leakage current errors, noise pick-up, and gain peaking as a result of stray capacitance. Output voltage increases linearly with light intensity. The amplifier is designed for single or dual power-supply operation.

The 0.09 inch × 0.09 inch (2.29 mm × 2.29 mm) photodiode operates in the photoconductive mode for excellent linearity and low dark current.

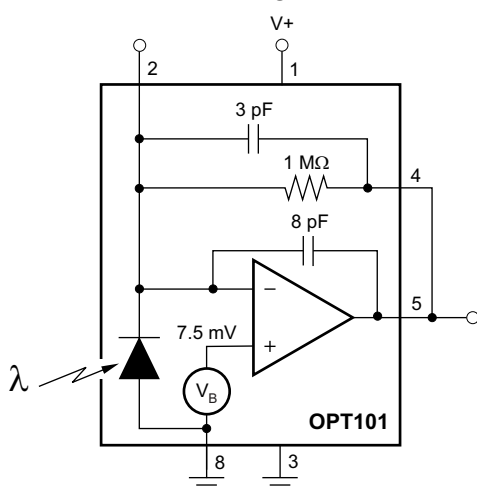
The OPT101 operates from 2.7 V to 36 V supplies and quiescent current is only 120  $\mu\text{A}$ . This device is available in clear plastic 8-pin PDIP, and J-lead SOP for surface mounting. The temperature range is 0°C to 70°C.

### Device Information<sup>(1)</sup>

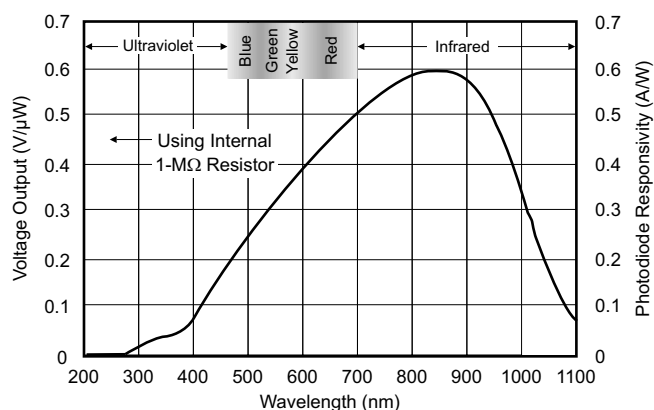
| PART NUMBER | PACKAGE  | BODY SIZE (NOM)   |
|-------------|----------|-------------------|
| OPT101      | PDIP (8) | 9.53 mm × 6.52 mm |
|             | SOP (8)  | 9.52 mm × 6.52 mm |

(1) For all available packages, see the package option addendum at the end of the data sheet.

### Block Diagram



### Spectral Responsivity



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## 4 Revision History

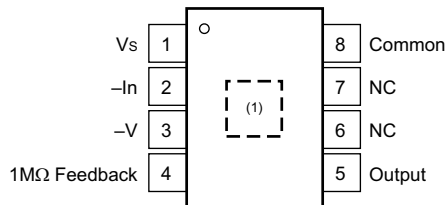
### Changes from Revision A (October 2003) to Revision B

Page

|                                                                                                                                                                                                                                                                                                                                                                                                     |           |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------|
| • Added <i>Pin Functions</i> , <i>ESD Ratings</i> , <i>Recommended Operating Conditions</i> , and <i>Thermal information</i> tables, and <i>Parameter Measurement Information</i> , <i>Detailed Description</i> , <i>Application and Implementation</i> , <i>Power-Supply Recommendations</i> , <i>Layout</i> , and <i>Device and Documentation Support</i> sections; moved existing sections ..... | <b>1</b>  |
| • Deleted W version of device from Tolerance parameter of Electrical Characteristics table; W version now obsolete .....                                                                                                                                                                                                                                                                            | <b>5</b>  |
| • Changed <i>Application Information</i> section .....                                                                                                                                                                                                                                                                                                                                              | <b>16</b> |

## 5 Pin Configuration and Functions

**DTL and NTC Packages  
8-pin SOP and 8-pin PDIP  
Top View**



(1) Photodiode location.

**Pin Functions**

| PIN |                | I/O    | DESCRIPTION                                                                                                             |
|-----|----------------|--------|-------------------------------------------------------------------------------------------------------------------------|
| NO. | NAME           |        |                                                                                                                         |
| 1   | V <sub>S</sub> | Power  | Power supply of device. Apply 2.7 V to 36 V relative to –V pin.                                                         |
| 2   | –In            | Input  | Negative input of op amp and the cathode of the photodiode. Either do not connect, or apply additional op amp feedback. |
| 3   | –V             | Power  | Most negative power supply. Connect to ground or a negative voltage that meets the recommended operating conditions.    |
| 4   | 1MΩ Feedback   | Input  | Connection to internal feedback network. Typically connect to Output, pin 5.                                            |
| 5   | Output         | Output | Output of device.                                                                                                       |
| 6   | NC             | —      | Do not connect                                                                                                          |
| 7   | NC             | —      | Do not connect                                                                                                          |
| 8   | Common         | Input  | Anode of the photodiode. Typically, connect to ground.                                                                  |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

|                                                   |                    | MIN        | MAX | UNIT |
|---------------------------------------------------|--------------------|------------|-----|------|
| Supply voltage ( $V_S$ to Common pin or $-V$ pin) |                    | 0          | 36  | V    |
| Output short-circuit (to ground)                  |                    | Continuous |     |      |
| Temperature                                       | Operating          | –25        | 85  | °C   |
|                                                   | Junction           |            | 85  | °C   |
|                                                   | Storage, $T_{stg}$ | –25        | 85  | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|                                     |                                                                                | VALUE | UNIT |
|-------------------------------------|--------------------------------------------------------------------------------|-------|------|
| $V_{(ESD)}$ Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>              | ±2000 | V    |
|                                     | Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup> | ±500  |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                     | MIN | NOM | MAX | UNIT |
|---------------------|-----|-----|-----|------|
| <b>POWER SUPPLY</b> |     |     |     |      |
| Operating voltage   | 2.7 |     | 36  | V    |
| <b>TEMPERATURE</b>  |     |     |     |      |
| Specified           | 0   |     | 70  | °C   |
| Operating           | 0   |     | 70  | °C   |

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |                                              | OPT101    |            | UNIT |
|-------------------------------|----------------------------------------------|-----------|------------|------|
|                               |                                              | DTL (SOP) | NTC (PDIP) |      |
|                               |                                              | 8 PINS    | 8 PINS     |      |
| $R_{\theta JA}$               | Junction-to-ambient thermal resistance       | 138.6     | 128.2      | °C/W |
| $R_{\theta JC(top)}$          | Junction-to-case (top) thermal resistance    | 96.4      | 113.1      | °C/W |
| $R_{\theta JB}$               | Junction-to-board thermal resistance         | 126.6     | 107.0      | °C/W |
| $\Psi_{JT}$                   | Junction-to-top characterization parameter   | 17.8      | 24.2       | °C/W |
| $\Psi_{JB}$                   | Junction-to-board characterization parameter | 118.8     | 105.9      | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 2.7\text{ V}$  to  $36\text{ V}$ ,  $\lambda = 650\text{ nm}$ , internal  $1\text{-M}\Omega$  feedback resistor, and  $R_L = 10\text{ k}\Omega$  (unless otherwise noted)

| PARAMETER                             | TEST CONDITIONS                                                                            | MIN           | TYP            | MAX       | UNIT                         |
|---------------------------------------|--------------------------------------------------------------------------------------------|---------------|----------------|-----------|------------------------------|
| <b>RESPONSIVITY</b>                   |                                                                                            |               |                |           |                              |
| Photodiode current                    |                                                                                            |               | 0.45           |           | A/W                          |
| Voltage output                        |                                                                                            |               | 0.45           |           | V/ $\mu\text{W}$             |
| Voltage output vs temperature         |                                                                                            |               | 100            |           | ppm/ $^\circ\text{C}$        |
| Unit-to-unit variation                |                                                                                            |               | $\pm 5\%$      |           |                              |
| Nonlinearity <sup>(1)</sup>           | Full-scale (FS) output = $24\text{ V}$                                                     |               | $\pm 0.01$     |           | % of FS                      |
| Photodiode area                       | $0.090\text{ in} \times 0.090\text{ in}$                                                   |               | 0.008          |           | $\text{in}^2$                |
|                                       | $2.29\text{ mm} \times 2.29\text{ mm}$                                                     |               | 5.2            |           | $\text{mm}^2$                |
| <b>DARK ERRORS, RTO<sup>(2)</sup></b> |                                                                                            |               |                |           |                              |
| Offset voltage, output                |                                                                                            | 5             | 7.5            | 10        | mV                           |
| Offset voltage vs temperature         |                                                                                            |               | $\pm 10$       |           | $\mu\text{V}/^\circ\text{C}$ |
| Offset voltage vs power supply        | $V_S = 2.7\text{ V}$ to $36\text{ V}$                                                      |               | 10             | 100       | $\mu\text{V}/\text{V}$       |
| Voltage noise, dark                   | $f_B = 0.1\text{ Hz}$ to $20\text{ kHz}$ , $V_S = 15\text{ V}$ , $V_{PIN3} = -15\text{ V}$ |               | 300            |           | $\mu\text{Vrms}$             |
| <b>TRANSIMPEDANCE GAIN</b>            |                                                                                            |               |                |           |                              |
| Resistor                              |                                                                                            |               | 1              |           | $\text{M}\Omega$             |
| Tolerance                             |                                                                                            |               | $\pm 0.5\%$    | $\pm 2\%$ |                              |
| Tolerance vs temperature              |                                                                                            |               | $\pm 50$       |           | ppm/ $^\circ\text{C}$        |
| <b>FREQUENCY RESPONSE</b>             |                                                                                            |               |                |           |                              |
| Bandwidth                             | $V_{OUT} = 10\text{ V}_{PP}$                                                               |               | 14             |           | kHz                          |
| Rise and fall time                    | 10% to 90%, $V_{OUT} = 10\text{-V}$ step                                                   |               | 28             |           | $\mu\text{s}$                |
| Settling time                         | to 0.05%, $V_{OUT} = 10\text{-V}$ step                                                     |               | 160            |           | $\mu\text{s}$                |
|                                       | to 0.1%, $V_{OUT} = 10\text{-V}$ step                                                      |               | 80             |           | $\mu\text{s}$                |
|                                       | to 1%, $V_{OUT} = 10\text{-V}$ step                                                        |               | 70             |           | $\mu\text{s}$                |
| Overload recovery                     | 100%, return to linear operation                                                           |               | 50             |           | $\mu\text{s}$                |
| <b>OUTPUT</b>                         |                                                                                            |               |                |           |                              |
| Voltage output, high                  |                                                                                            | $(V_S) - 1.3$ | $(V_S) - 1.15$ |           | V                            |
| Capacitive load, stable operation     |                                                                                            |               | 10             |           | nF                           |
| Short-circuit current                 | $V_S = 36\text{ V}$                                                                        |               | 15             |           | mA                           |
| <b>POWER SUPPLY</b>                   |                                                                                            |               |                |           |                              |
| Quiescent current                     | Dark, $V_{PIN3} = 0\text{ V}$                                                              |               | 120            |           | $\mu\text{A}$                |
|                                       | $R_L = \infty$ , $V_{OUT} = 10\text{ V}$                                                   |               | 220            |           | $\mu\text{A}$                |

(1) Deviation in percent of full scale from best-fit straight line.

(2) Referred to output. Includes all error sources.

## 6.6 Electrical Characteristics: Photodiode

At  $T_A = 25^\circ\text{C}$  and  $V_S = 2.7\text{ V}$  to  $36\text{ V}$  (unless otherwise noted)

| PARAMETER                   | TEST CONDITIONS                    | MIN                             | TYP   | MAX | UNIT                                |
|-----------------------------|------------------------------------|---------------------------------|-------|-----|-------------------------------------|
| Photodiode area             | 0.090 in $\times$ 0.090 in         |                                 | 0.008 |     | in <sup>2</sup>                     |
|                             | 2.29 mm $\times$ 2.29 mm           |                                 | 5.2   |     | mm <sup>2</sup>                     |
| Current responsivity        | $\lambda = 650\text{ nm}$          |                                 | 0.45  |     | A/W                                 |
|                             |                                    |                                 | 865   |     | ( $\mu\text{A/W}$ )/cm <sup>2</sup> |
| Dark current                | $V_{\text{DIODE}} = 7.5\text{ mV}$ |                                 | 2.5   |     | pA                                  |
| Dark current vs temperature | $V_{\text{DIODE}} = 7.5\text{ mV}$ | Doubles every $7^\circ\text{C}$ |       |     | —                                   |
| Capacitance                 |                                    |                                 | 1200  |     | pF                                  |

## 6.7 Electrical Characteristics: Op Amp<sup>(1)</sup>

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 2.7\text{ V}$  to  $36\text{ V}$ ,  $\lambda = 650\text{ nm}$ , internal 1-M $\Omega$  feedback resistor, and  $R_L = 10\text{ k}\Omega$  (unless otherwise noted)

| PARAMETER                             | TEST CONDITIONS                                 | MIN                              | TYP                | MAX | UNIT                         |
|---------------------------------------|-------------------------------------------------|----------------------------------|--------------------|-----|------------------------------|
| <b>INPUT</b>                          |                                                 |                                  |                    |     |                              |
| Offset voltage                        |                                                 |                                  | $\pm 0.5$          |     | mV                           |
| vs temperature                        |                                                 |                                  | $\pm 2.5$          |     | $\mu\text{V}/^\circ\text{C}$ |
| vs power supply                       |                                                 |                                  | 10                 |     | $\mu\text{V/V}$              |
| Input bias current                    | (–) input                                       |                                  | 165                |     | pA                           |
| vs temperature                        | (–) input                                       | Doubles every $10^\circ\text{C}$ |                    |     | —                            |
| Input impedance                       | Differential                                    |                                  | 400    5           |     | M $\Omega$    pF             |
|                                       | Common-mode                                     |                                  | 250    35          |     | G $\Omega$    pF             |
| Common-mode input voltage range       | Linear operation                                |                                  | 0 to ( $V_S - 1$ ) |     | V                            |
| Common-mode rejection                 |                                                 |                                  | 90                 |     | dB                           |
| <b>OPEN-LOOP GAIN</b>                 |                                                 |                                  |                    |     |                              |
| Open-loop voltage gain                |                                                 |                                  | 90                 |     | dB                           |
| <b>FREQUENCY RESPONSE</b>             |                                                 |                                  |                    |     |                              |
| Gain bandwidth product <sup>(2)</sup> |                                                 |                                  | 2                  |     | MHz                          |
| Slew rate                             |                                                 |                                  | 1                  |     | V/ $\mu\text{s}$             |
| Settling time                         | 0.05%                                           |                                  | 8.0                |     | $\mu\text{s}$                |
|                                       | 0.1%                                            |                                  | 7.7                |     | $\mu\text{s}$                |
|                                       | 1%                                              |                                  | 5.8                |     | $\mu\text{s}$                |
| <b>OUTPUT</b>                         |                                                 |                                  |                    |     |                              |
| Voltage output, high                  |                                                 | $(V_S) - 1.3$ $(V_S) - 1.15$     |                    |     | V                            |
| Short-circuit current                 | $V_S = 36\text{ V}$                             |                                  | 15                 |     | mA                           |
| <b>POWER SUPPLY</b>                   |                                                 |                                  |                    |     |                              |
| Quiescent current                     | Dark, $V_{\text{PIN3}} = 0\text{ V}$            |                                  | 120                |     | $\mu\text{A}$                |
|                                       | $R_L = \infty$ , $V_{\text{OUT}} = 10\text{ V}$ |                                  | 220                |     | $\mu\text{A}$                |

(1) Op amp specifications provided for information and comparison only.

(2) Stable gains  $\geq 10\text{ V/V}$ .

## 6.8 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 2.7\text{ V}$  to  $36\text{ V}$ ,  $\lambda = 650\text{ nm}$ , internal  $1\text{-M}\Omega$  feedback resistor, and  $R_L = 10\text{ k}\Omega$  (unless otherwise noted)

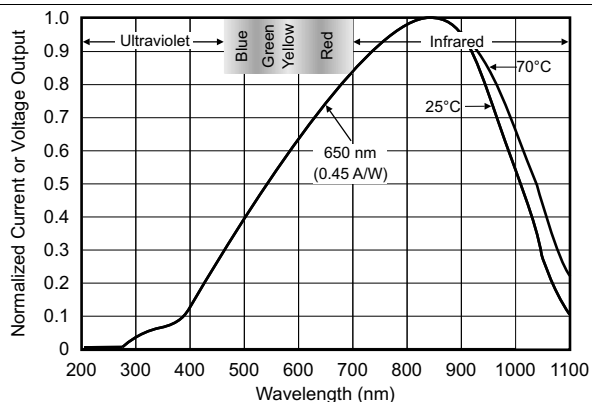


Figure 1. Normalized Spectral Responsivity

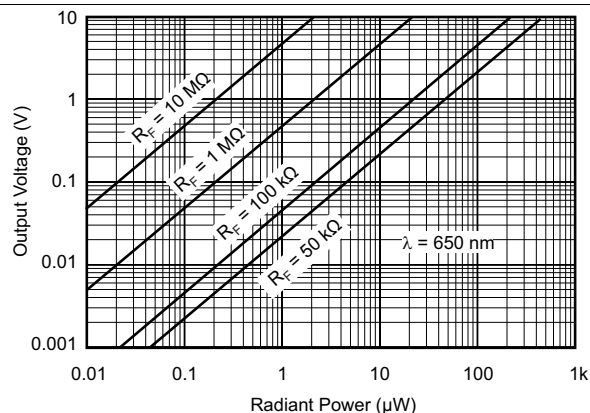


Figure 2. Voltage Responsivity vs Radiant Power

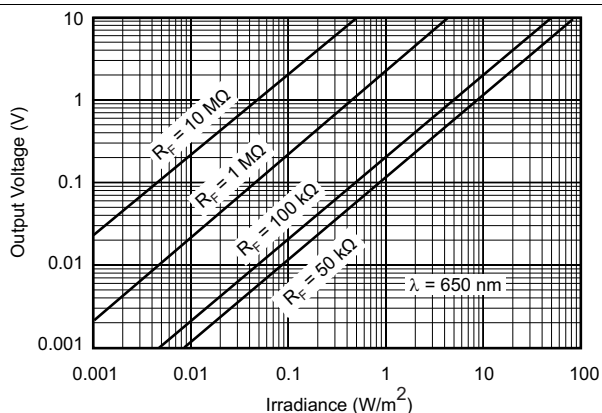


Figure 3. Voltage Responsivity vs Irradiance

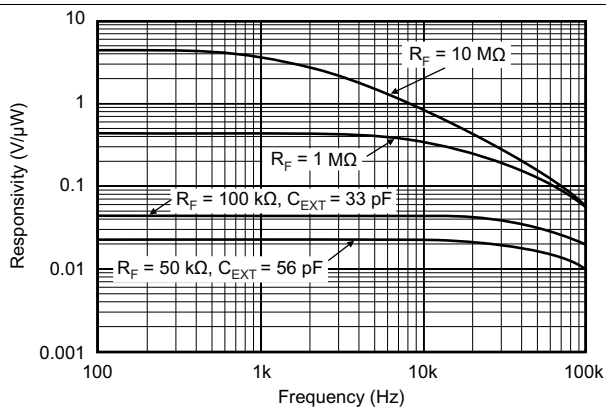


Figure 4. Voltage Responsivity vs Frequency

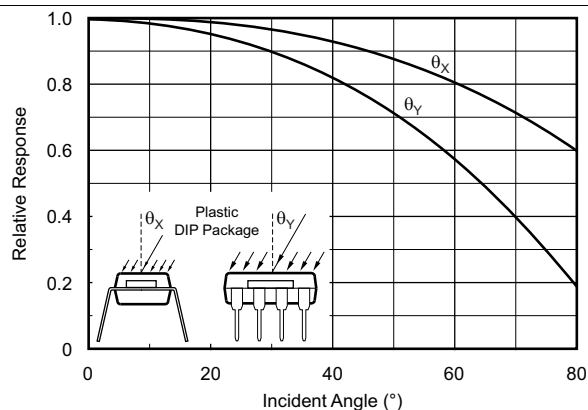


Figure 5. Response vs Incident Angle

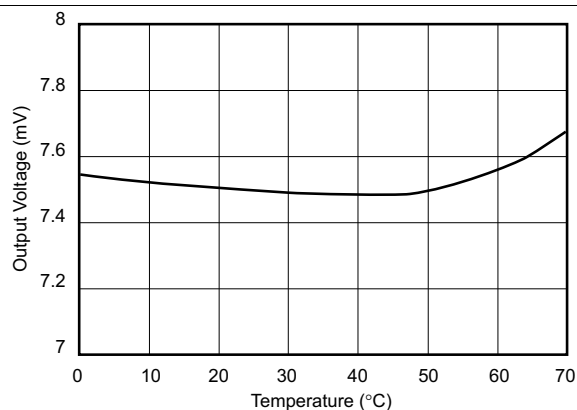


Figure 6. Dark  $V_{OUT}$  vs Temperature

## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 2.7\text{ V}$  to  $36\text{ V}$ ,  $\lambda = 650\text{ nm}$ , internal  $1\text{-M}\Omega$  feedback resistor, and  $R_L = 10\text{ k}\Omega$  (unless otherwise noted)

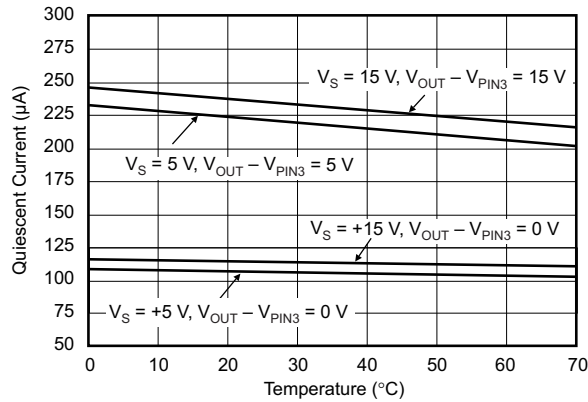


Figure 7. Quiescent Current vs Temperature

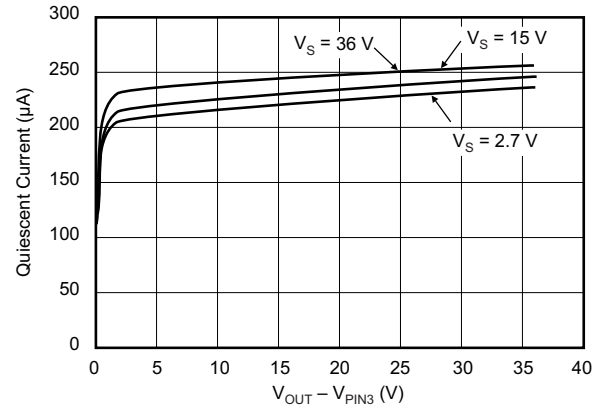


Figure 8. Quiescent Current vs ( $V_{OUT} - V_{PIN3}$ )

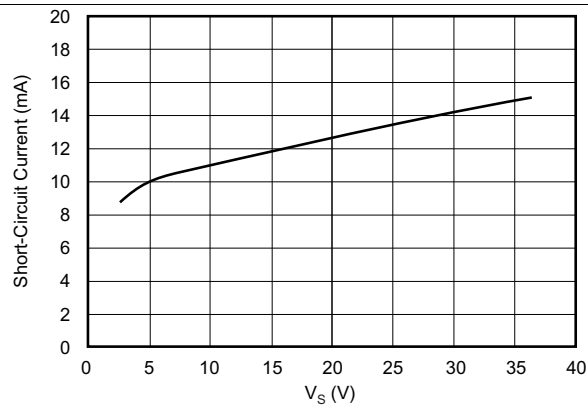


Figure 9. Short-Circuit Current vs  $V_S$

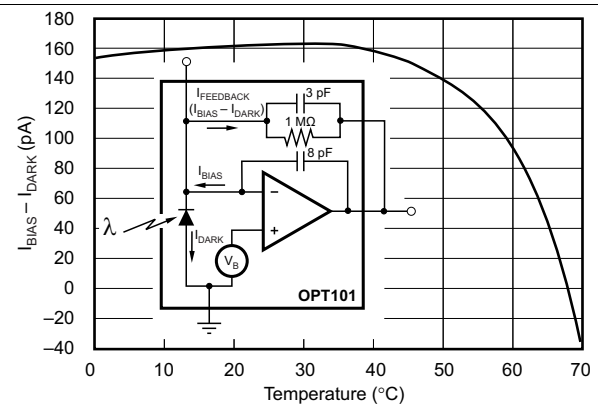


Figure 10. ( $I_{BIAS} - I_{DARK}$ ) vs Temperature

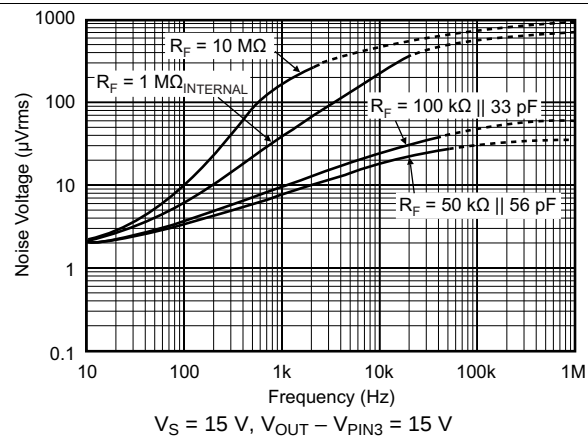


Figure 11. Output Noise Voltage vs Measurement Bandwidth

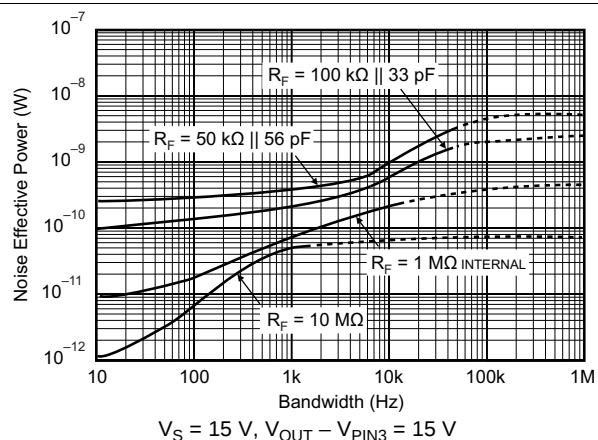


Figure 12. Noise Effective Power vs Measurement Bandwidth

## Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = 2.7\text{ V}$  to  $36\text{ V}$ ,  $\lambda = 650\text{ nm}$ , internal  $1\text{-M}\Omega$  feedback resistor, and  $R_L = 10\text{ k}\Omega$  (unless otherwise noted)

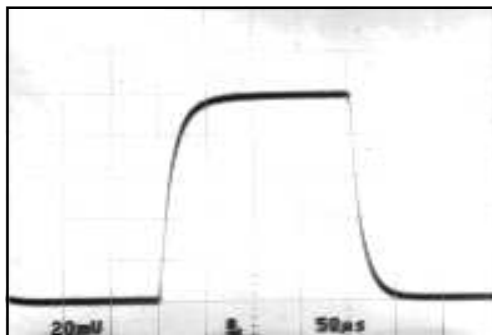
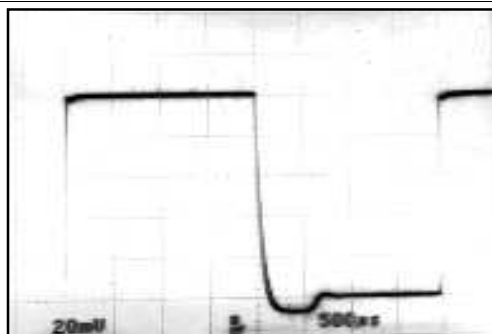


Figure 13. Small-Signal Response

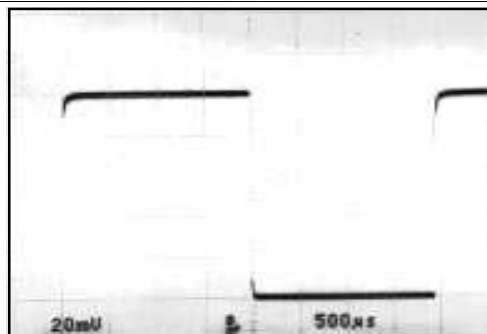


Figure 14. Large-Signal Response



$C_{\text{LOAD}} = 10,000\text{ pF}$ , pin 3 =  $0\text{ V}$

Figure 15. Small-Signal Response



$C_{\text{LOAD}} = 10,000\text{ pF}$ , Pin 3 =  $-15\text{ V}$

Figure 16. Small-Signal Response

## 7 Parameter Measurement Information

### 7.1 Light Source Positioning and Uniformity

The OPT101 is tested with a light source that uniformly illuminates the full area of the integrated circuit, including the op amp. Although the silicon of integrated circuit (IC) amplifiers is light-sensitive to some degree, the OPT101 op amp circuitry is designed to minimize this effect. Sensitive junctions are shielded with metal, and the photodiode area is very large relative to the op amp input circuitry.

If the light source is focused to a small area, be sure that it is properly aimed to fall on the photodiode. A narrowly-focused beam falling only on the photodiode provides improved settling times compared to a source that uniformly illuminates the full area of the die. If a narrowly-focused light source misses the photodiode area and falls only on the op amp circuitry, the OPT101 does not perform properly. The large 0.09-in × 0.09-in (2.29 mm × 2.29 mm) photodiode area allows easy positioning of narrowly-focused light sources. The photodiode area is easily visible because the area appears very dark compared to the surrounding active circuitry.

The incident angle of the light source also effects the apparent sensitivity in uniform irradiance. For small incident angles, the loss in sensitivity is simply due to the smaller effective light gathering area of the photodiode (proportional to the cosine of the angle). At a greater incident angle, light is diffracted and scattered by the package. These effects are shown in [Figure 5](#).

## 8 Detailed Description

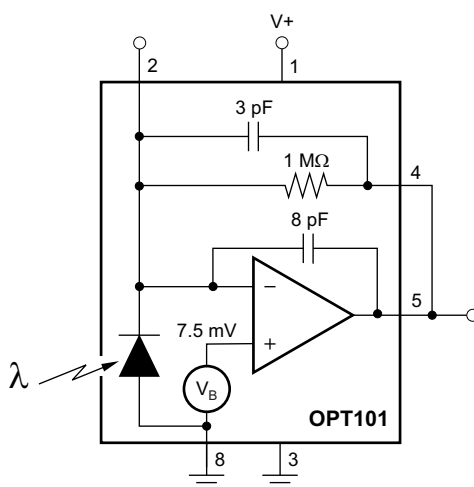
### 8.1 Overview

The OPT101 is a large-area photodiode integrated with an optimized operational amplifier that makes the OPT101 a small, easy-to-use, light-to-voltage device. The photodiode has a very large measurement area that collects a significant amount of light, and thus allows for high-sensitivity measurements. The photodiode has a wide spectral response with a maximum peak in the infrared spectrum, and a useable range from 300 nm to 1100 nm. The wide power-supply range of 2.7 V to 36 V makes this device useful in a variety of architectures; from all-analog circuits to data conversion base circuits. The on-chip voltage source keeps the amplifier in a good operating region, even at low light levels.

The OPT101 voltage output is the product of the photodiode current times the feedback resistor, ( $I_D R_F$ ), plus a pedestal voltage,  $V_B$ , of approximately 7.5 mV introduced for single-supply operation. Output is 7.5 mV dc with no light, and increases with increasing illumination. Photodiode current,  $I_D$ , is proportional to the radiant power, or flux, (in watts) falling on the photodiode. At a wavelength of 650 nm (visible red) the photodiode responsivity,  $R_I$ , is approximately 0.45 A/W. Responsivity at other wavelengths is shown in [Figure 1](#). The internal feedback resistor is laser trimmed to 1 MΩ. Using this resistor, the output voltage responsivity,  $R_V$ , is approximately 0.45 V/μW at 650-nm wavelength.

See [Figure 2](#) for the response throughout a wide range of radiant power in microwatts. [Figure 3](#) shows the response throughout a wide range of irradiance in watts per square meter.

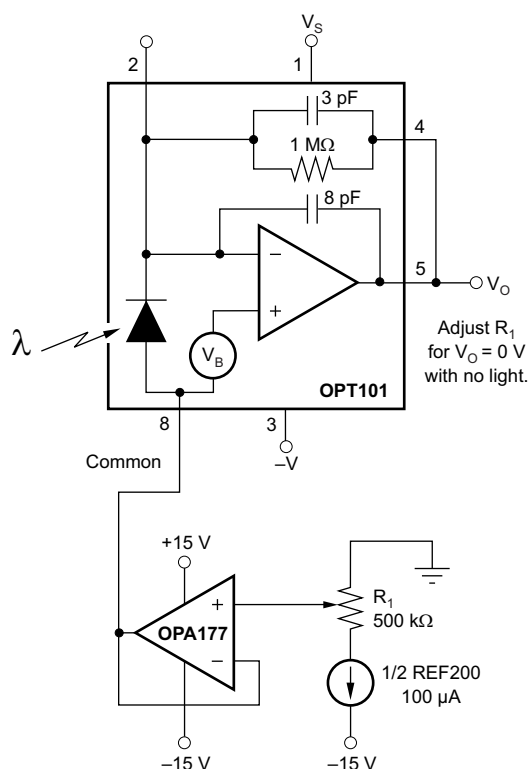
### 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Dark Performance

The dark errors in the [Electrical Characteristics](#) table include all sources. The dominant source of dark output voltage is the pedestal voltage applied to the noninverting input of the op amp. This voltage is introduced to provide linear operation in the absence of light falling on the photodiode. Photodiode dark current is approximately 2.5 pA, and contributes virtually no offset error at room temperature. The bias current of the op amp summing junction (negative input) is approximately 165 pA. The dark current is subtracted from the amplifier bias current, and this residual current flows through the feedback resistor creating an offset. The effects of temperature on this difference current are seen in [Figure 10](#). The dark output voltage is trimmed to zero with the optional circuit shown in [Figure 17](#). Use a low-impedance offset driver (op amp) to drive pin 8 (Common) because this node has signal-dependent currents.



**Figure 17. Dark Error (Offset) Adjustment Circuit**

## Feature Description (continued)

### 8.3.2 Feedback Network and Dynamic Response

The OPT101 features a feedback network for optimal dynamic response. The dynamic response of the OPT101 is dominated by the feedback network and op amp combination. Using the internal 1-M $\Omega$  resistor, the dynamic response of the photodiode and op amp combination can be modeled as a simple RC circuit with a –3-dB cutoff frequency of approximately 14 kHz. The R and C values are 1 M $\Omega$  and 11 pF, respectively. To improve the frequency response, use external resistors with less than 3-pF parasitic capacitance. An external 1-M $\Omega$  resistor used in the configuration shown in Figure 19 creates a 23-kHz bandwidth with the same 106 V/A dc transimpedance gain. This increased bandwidth yields a rise time of approximately 15  $\mu$ s (10% to 90%). Dynamic response is not limited by op amp slew rate, as demonstrated in Figure 13 and Figure 14, showing virtually identical large-signal and small-signal response.

Dynamic response varies with feedback network value, as shown in Figure 4. Rise time (10% to 90%) varies as a function of the –3-dB bandwidth produced by the feedback network value shown in Equation 1:

$$t_r = 0.35 / f_c$$

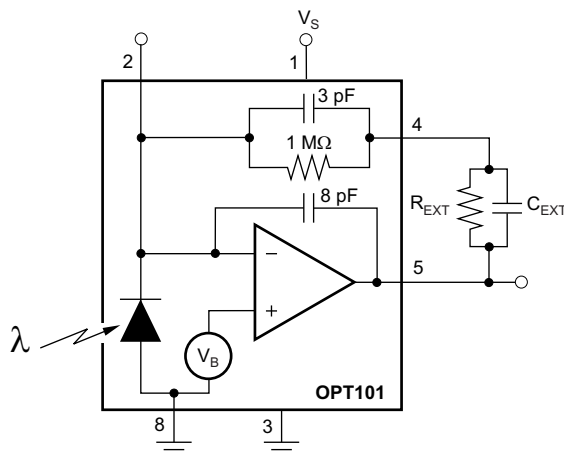
where

- $t_r$  is the rise time (10% to 90%)
- $f_c$  is the –3dB bandwidth

(1)

#### 8.3.2.1 Changing Responsivity

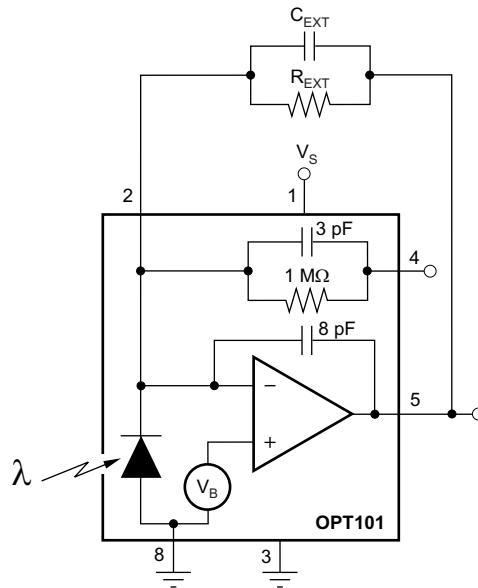
To set a different voltage responsivity, connect an external resistor,  $R_{EXT}$ . To increase the responsivity, place this resistor in series with the internal 1-M $\Omega$  resistor (Figure 18), or replace the internal resistor with an external resistor by not connecting pin 4 (Figure 19). The second configuration also reduces the circuit gain below 106 V/A when using external resistors that are less than 1 M $\Omega$ .



**Figure 18. Changing Responsivity with External Resistor in Series with Internal Resistor**

**Table 1. Responsivity and Bandwidth for Figure 18**

| $R_{EXT}$<br>(M $\Omega$ ) | $C_{EXT}$<br>(pF) | DC Gain<br>( $\times 10^6$ V/A) | Bandwidth<br>(kHz) |
|----------------------------|-------------------|---------------------------------|--------------------|
| 1                          | 50                | 2                               | 8                  |
| 2                          | 25                | 3                               | 6                  |
| 5                          | 10                | 6                               | 2.5                |
| 10                         | 5                 | 11                              | 1.3                |
| 50                         | —                 | 51                              | 0.33               |



**Figure 19. Changing Responsivity with External Resistor Only (Internal Resistor Disabled)**

**Table 2. Responsivity and Bandwidth for Figure 19**

| $R_{EXT}$<br>(MΩ)   | $C_{EXT}$<br>(pF) | DC Gain<br>( $\times 10^6 V/A$ ) | Bandwidth<br>(kHz) |
|---------------------|-------------------|----------------------------------|--------------------|
| 0.05 <sup>(1)</sup> | 56                | 0.05                             | 58                 |
| 0.1 <sup>(1)</sup>  | 33                | 0.1                              | 44                 |
| 1                   | —                 | 1                                | 23                 |
| 2                   | —                 | 2                                | 9.4                |
| 5                   | —                 | 5                                | 3.6                |
| 10                  | —                 | 10                               | 1.8                |
| 50                  | —                 | 50                               | 0.34               |

(1) May require 1 kΩ in series with pin 5 when driving large capacitances.

Applications using a feedback resistor significantly larger than the internal 1-MΩ resistor require special consideration. Input bias current of the op amp and dark current of the photodiode increase significantly at higher temperatures. This increase combined with the higher gain ( $R_F > 1 \text{ M}\Omega$ ) can cause the op amp output to be driven to ground at high temperatures. If this problem occurs, use a positive bias voltage applied to pin 8 to make sure that the op amp output remains in the linear operating region when the photodiode is not exposed to light. Alternatively, use a dual power supply. The output may be negative when sensing dark conditions. Use the information discussed in the [Dark Performance](#) section and [Figure 10](#) to analyze the desired configuration.

### 8.3.3 Noise Performance

Noise performance of the OPT101 is determined by the op amp characteristics, feedback network, photodiode capacitance, and signal level. [Figure 11](#) shows how the noise varies with  $R_F$  and measured bandwidth (0.1 Hz to the indicated frequency), when the output voltage minus the voltage on pin 3 ( $-V$ ) is greater than approximately 50 mV. Below this level, the output stage is powered down, and the effective bandwidth is decreased. This decreased bandwidth reduces the noise to approximately 1/3 the nominal noise value of 300  $\mu V_{rms}$ , or 100  $\mu V_{rms}$ . This decreased bandwidth enables a low-level signal to be resolved.

To reduce noise and improve the signal-to-noise ratio, filter the output with a cutoff frequency equal to the signal bandwidth. In addition, output noise increases in proportion to the square root of the feedback resistance, while responsivity increases linearly with feedback resistance. To improve the signal-to-noise ratio performance, use large feedback resistance, if decreased bandwidth is acceptable to the application.

The noise performance of the photodetector is sometimes characterized by noise effective power (NEP), the radiant power that produces an output signal equal to the noise level. NEP has the units of radiant power (watts), or  $W/\sqrt{\text{Hz}}$  to convey spectral information about the noise. Figure 12 illustrates the NEP for the OPT101.

### 8.3.4 Linearity Performance

The photodiode is operated in the photoconductive mode so the current output of the photodiode is very linear with radiant power throughout a wide range. Nonlinearity remains less than approximately 0.05% for photodiode currents less than 100- $\mu\text{A}$ . The photodiode is able to produce output currents of 1 mA or greater with high radiant power, but nonlinearity increases to several percent in this region.

This very linear performance at high radiant power assumes that the full photodiode area is uniformly illuminated. If the light source is focused to a small area of the photodiode, nonlinearity occurs at lower radiant power.

### 8.3.5 Capacitive Load Drive

The OPT101 is capable of driving load capacitances of 10 nF without instability. However, dynamic performance with capacitive loads may improve by applying a negative bias voltage to pin 3 ( $-V$ , shown in Figure 20). This negative power-supply voltage allows the output to go negative in response to the reactive effect of a capacitive load. An internal JFET connected between pin 5 (output) and pin 3 ( $-V$ ) allows the output to sink current. This current sink capability is also useful when driving the capacitive inputs of some analog-to-digital converters that require the signal source to sink currents up to approximately 100  $\mu\text{A}$ . The benefits of this current sink are shown in Figure 15 and Figure 16. These figures compare operation with pin 3 ( $-V$ ) grounded and connected to  $-15\text{ V}$ .

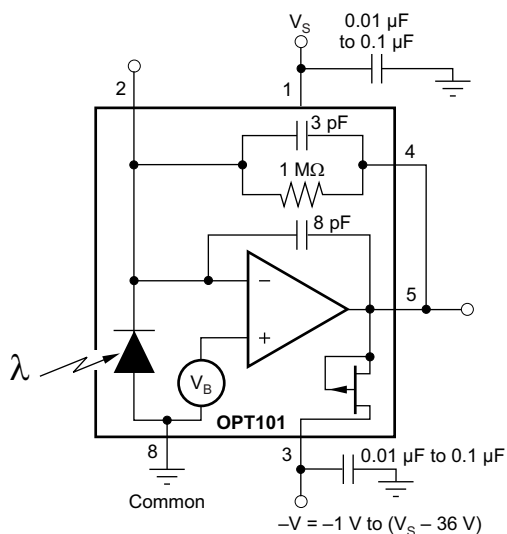


Figure 20. Bipolar Power-Supply Circuit Connections

Because of the architecture of this output stage current sink, there is a slight increase in operating current when there is a voltage between pin 3 ( $-V$ ) and the output. Depending on the magnitude of this voltage, the quiescent current increases by approximately 100  $\mu\text{A}$ , as shown in Figure 8.

## 8.4 Device Functional Modes

The OPT101 has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V. The maximum power supply voltage for the OPT101 is 36 V.

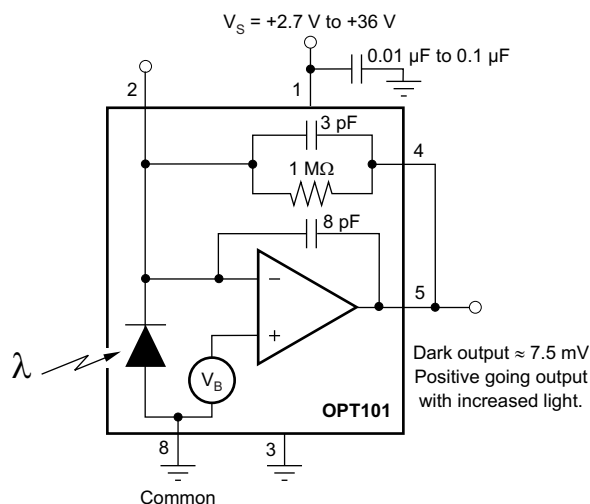
## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

Figure 21 shows the basic circuit connections for the OPT101 operating with a single power supply and using the internal 1-M $\Omega$  feedback resistor for a response of 0.45 V/ $\mu$ W at 650 nm. Pin 3 (–V) is connected to common in this configuration. Applications with high-impedance power supplies may require decoupling capacitors located close to the device pins as shown.



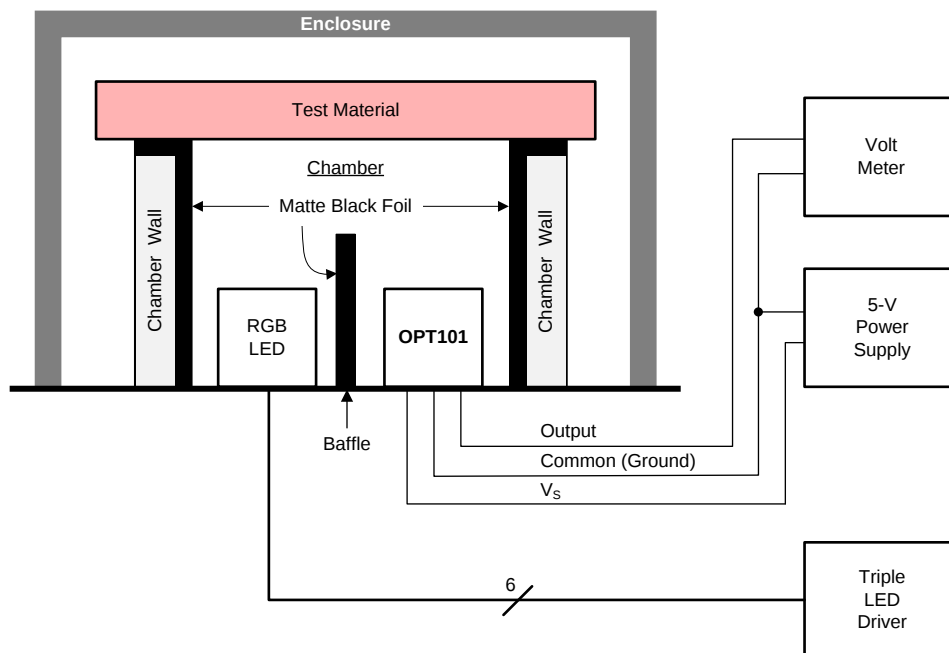
**Figure 21. Basic Circuit Connections**

## 9.2 Typical Applications

### 9.2.1 Color and Reflective Wavelength Tester

A common application for the OPT101 is testing physical materials. Information can be gained about a test material by determining the optical reflection, transmission, or absorption properties at particular wavelengths. These test materials can be solid objects, biological or chemical liquids, or any other type of material.

For an intuitive example, this application for OPT101 tests red, green, and blue reflective color properties of a variety of test materials. This application is not intended to match the color standards as defined by the Commission Internationale de l'Eclairage (CIE), but to illustrate a generic optical wavelength-specific test technique. Different applications can test for different wavelengths, including invisible ultraviolet or infrared wavelengths, that are appropriate for the objective of that application.



**Figure 22. Fixture for Measurement of Optical Reflective Properties of a Test Material**

#### 9.2.1.1 Design Requirements

For this design example, use the parameters listed in [Table 3](#) as the input design requirement parameters.

**Table 3. Design Parameters**

| DESIGN PARAMETER                                                   | VALUE      |
|--------------------------------------------------------------------|------------|
| Input power supply voltage                                         | 5 V        |
| Room ambient light condition                                       | < 2000 lux |
| Ratio of blue and green response to red response, for red target   | < 60%      |
| Ratio of red and green response to blue response, for blue target  | < 60%      |
| Ratio of red and blue response to green response, for green target | < 80%      |

### 9.2.1.2 Detailed Design Procedure

This design illuminates a test material with specific wavelengths, and measures the resulting reflection. Choose an RGB LED that sequentially creates individual red, green, and blue wavelengths. Red material has a strong reflection of red wavelengths, and a weaker reflection of green and blue wavelengths. Green and blue materials follow a similar pattern, reflecting the respective primary color wavelengths stronger than other color wavelengths.

Design a fixture with a chamber that allows the RGB LED to illuminate the test material and allows the OPT101 to receive the resulting reflection, as shown in [Figure 22](#). Design the chamber to keep out ambient light from the room. Line the chamber with a matte black foil so that the chamber walls absorb as much light as possible. The matte black foil helps the OPT101 sensor measure reflections primarily from the test material and only minimally from the chamber walls. Design a baffle structure between the RGB LED and the OPT101 sensor so that light does not transmit directly from the RGB LED to the OPT101 sensor without reflecting off of the test material. Place an additional enclosure over the chamber to enhance the isolation from any light in the room.

Drive the OPT101 power supply pin,  $V_S$ , with a 5-V power supply, and measure the output pin voltage with a voltmeter. This voltmeter can easily be replaced with an ADC.

Choose LED drive currents for each of the RGB LEDs. Throughout this procedure, either drive each LED with this specific chosen current, or do not drive the LED at all. Choose an LED drive current that equalizes the power dissipation (the drive current times the forward-biased voltage drop across each LED). This equal power dissipation minimizes thermal transient settling time when switching between the LEDs. This equal power dissipation is not a requirement if test speed and settling time are not an issue for the application.

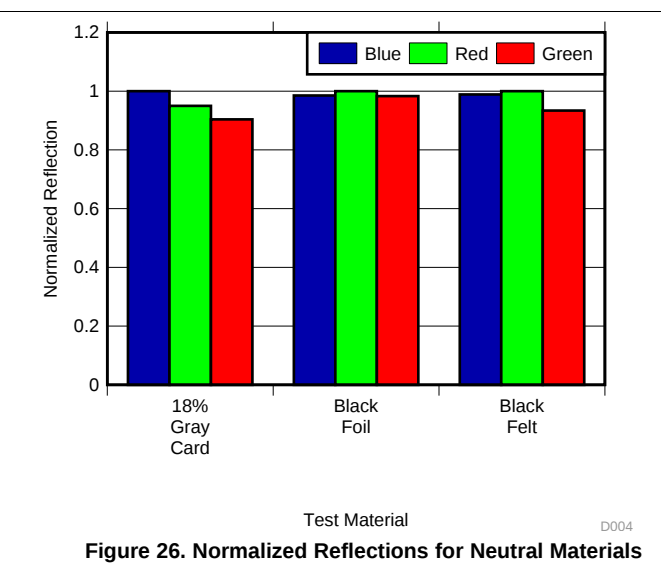
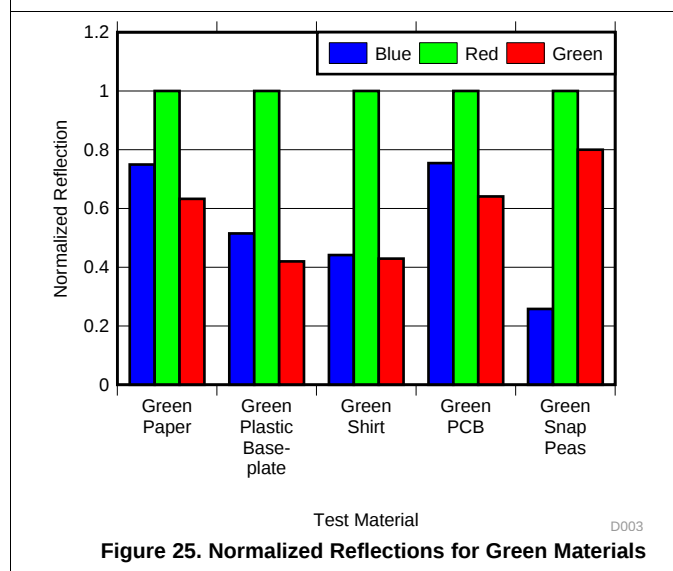
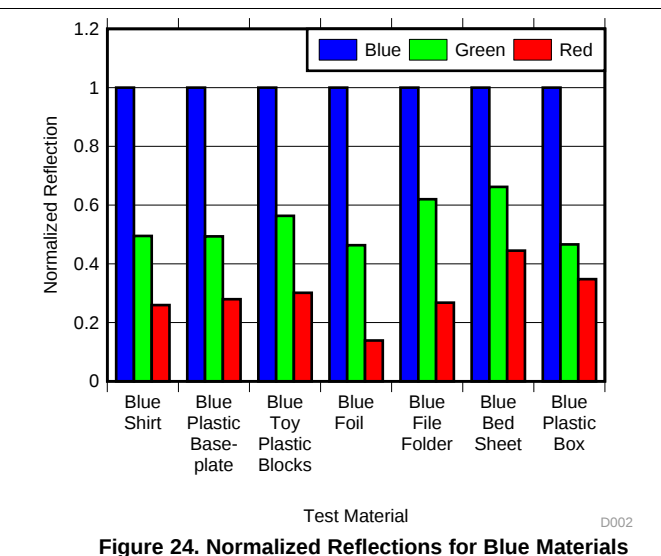
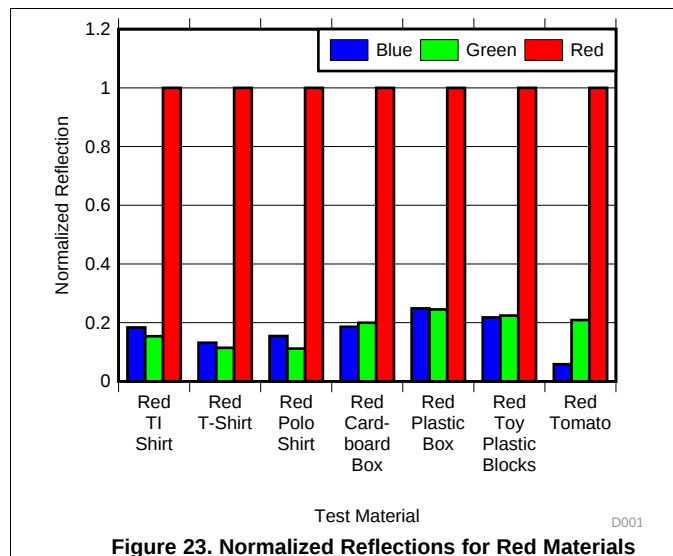
Calibrate the fixture by measuring a standard white card as a test material. Drive the red LED, and record the resulting voltage from the OPT101. Repeat this procedure with the green and blue LEDs.

Next, measure a test material with the same procedure used for the white card. Normalize the results by dividing the test material result by the white card result for each LED. Determine the color of the object by selecting the largest of the three LED normalized measurements. Perform an additional normalization step for data clarity by dividing each of the three LED measurements by the largest of the three measurements.

### 9.2.1.3 Application Curves

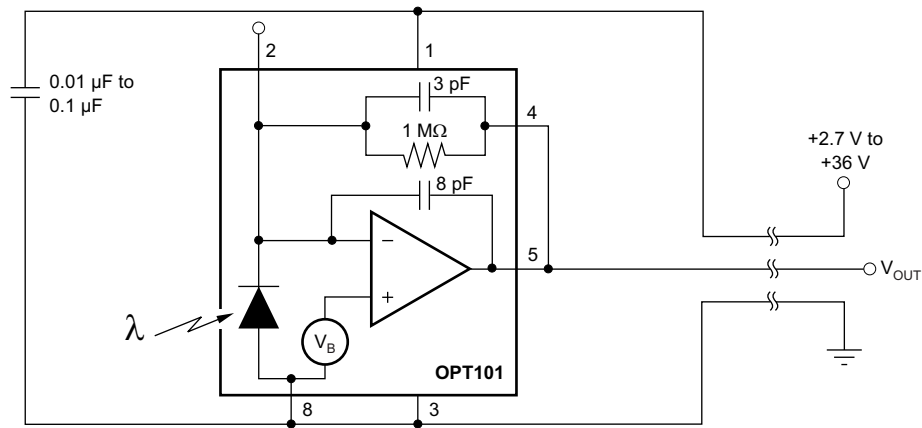
The following figures show that the colors of the test materials sorted properly, as expected. The red test materials all showed a stronger reflection for red LED than the green and blue LEDs. The results are plotted in four groups: red (Figure 23), blue (Figure 24), green (Figure 25), and neutral color (Figure 26). The application clearly identifies the primary color of each test material. When the color is neutral, then the red, green, and blue test results are very similar to each other, as expected (within 10% of each other).

The red results had the most contrast. The green results had the least contrast. These results are likely different because the red LED has the least spectral overlap with the green and blue LEDs. The green LED has the widest spectral content. If more contrast is required, try LEDs (or other light sources) with more-narrow spectrums.



### 9.2.2 Three-Wire Remote Light Measurement

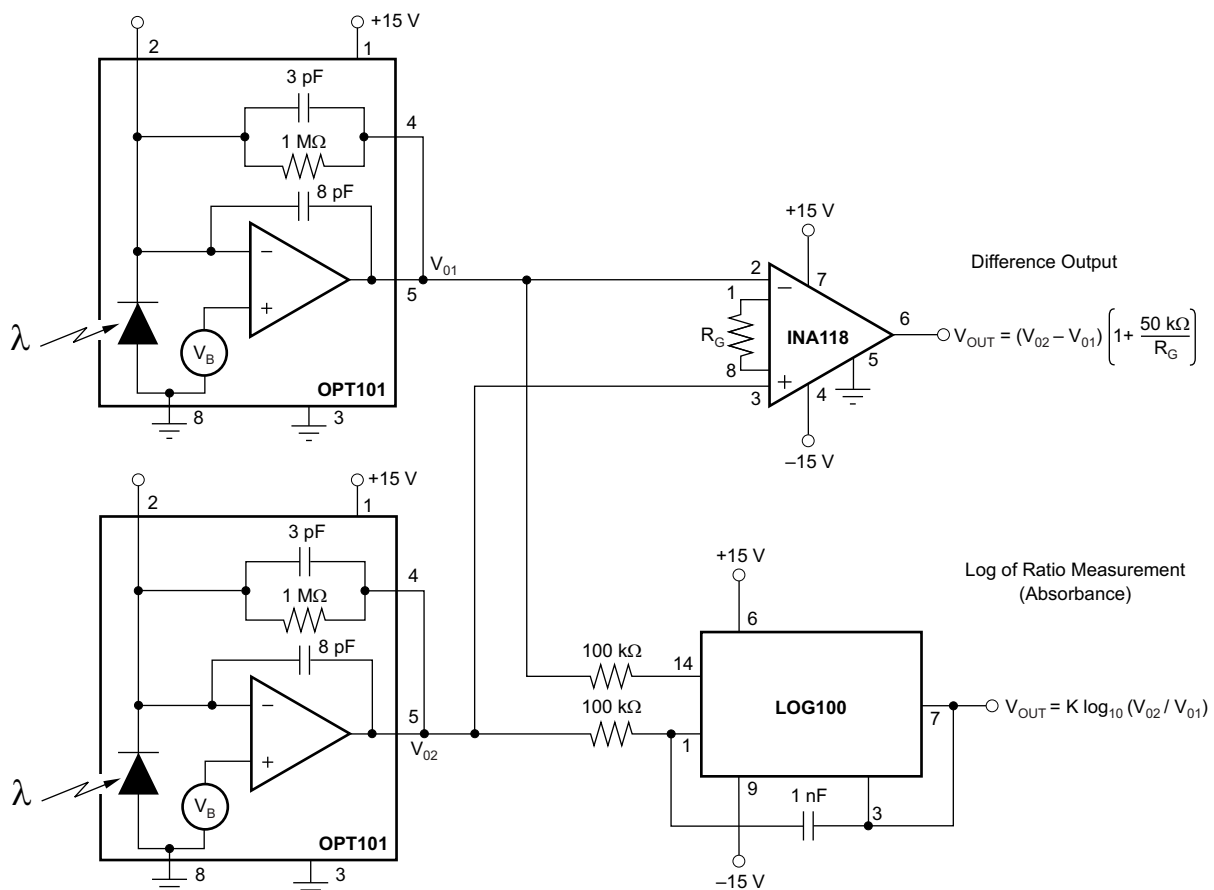
Use the connections to the OPT101 shown on the right side of [Figure 27](#) to sense a remote location with a three-wire light measurement circuit.



**Figure 27. Three-Wire Remote Light Measurement**

### 9.2.3 Differential Light Measurement

Use a configuration similar to [Figure 28](#) for applications that sense light gradients or differential light.



**Figure 28. Differential Light Measurement**

## 9.2.4 LED Output Regulation Circuit

To keep an LED (or other light) producing a constant amount of light over changing temperature and over the lifetime efficiency degradation of the LED, use a circuit similar to [Figure 29](#). As the efficiency of the LED degrades, this circuit increases the LED drive current to keep the output at the appropriate constant level.

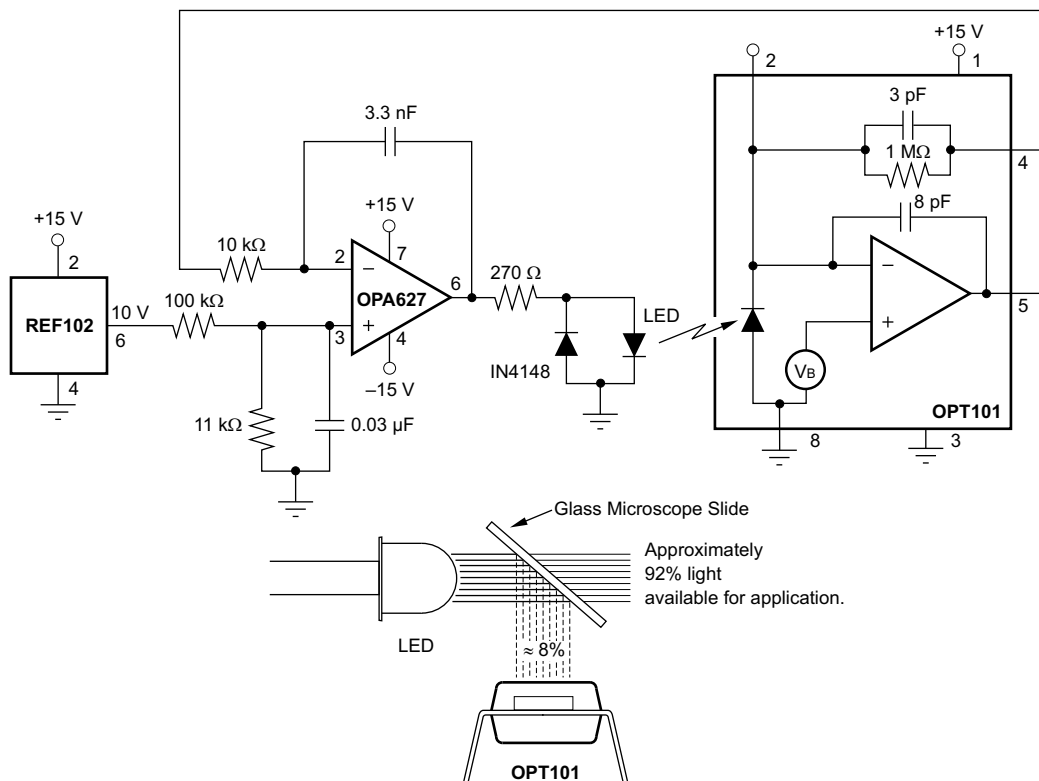


Figure 29. LED Output Regulation Circuit

### 9.3 Dos and Don'ts

As with any optical product, special care must be taken into consideration when handling the OPT101. Although the OPT101 has low sensitivity to dust and scratches, proper optical device handling procedures are still recommended.

The optical surface of the device must be kept clean for optimal performance in both prototyping with the device and mass production manufacturing procedures. Tweezers with plastic or rubber contact surfaces are recommended to avoid scratches on the optical surface. Avoid manipulation with metal tools when possible. The optical surface must be kept clean of fingerprints, dust, and other optical-inhibiting contaminants.

If the device optical surface requires cleaning, use deionized water or isopropyl alcohol. A few gentile brushes with a soft swab are appropriate. Avoid potentially abrasive cleaning and manipulating tools and excessive force that can scratch the optical surface.

If the OPT101 performs less than optimally, inspect the optical surface for dirt, scratches, or other optical artifacts.

Any light falling on the op amp circuitry area must be uniform; see the [Parameter Measurement Information](#) section for more information about light uniformity.

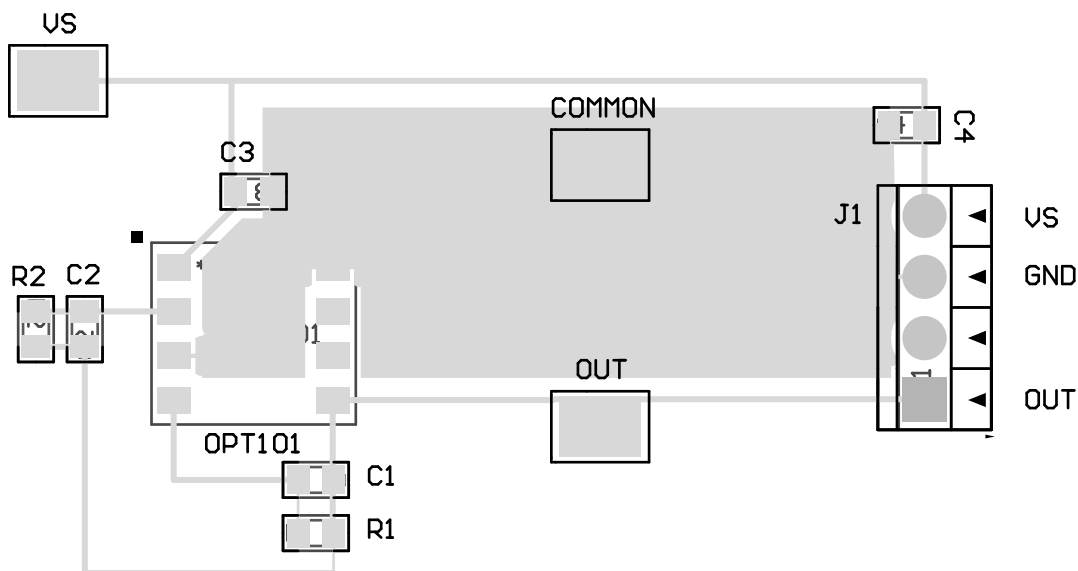
The OPT101 is designed to operate from an input voltage supply range between 2.7 V and 36 V. Make sure the power-supply input is well regulated. Place a 0.01- $\mu$ F to 0.1- $\mu$ F bypass capacitor with low-impedance, short connections between  $V_S$  (pin 1) and  $-V$  (pin 3). If  $-V$  (pin 3) is not connected to Common (pin 8), place an additional bypass capacitor between  $V_S$  (pin 1) and Common (pin 8).

## 11.1 Layout Guidelines

Depending on the application, the design might benefit from having the OPT101 mounted to the opposite side of the board as the other electrical components. Keeping the optical sensor side free from extra components allows for easier mounting of any required optical-mechanical structures around the OPT101.

## 11.2 Layout Example

The following example shows an external feedback network (R2 and C2) that bypasses the internal feedback network, similar to [Figure 19](#). This example also shows an external feedback network (R1, C1) in series with the internal feedback network, similar to [Figure 18](#). To use only the internal feedback network, load R1 or C1 with a short circuit. This example allows for three different configurations with the same layout. Do not load R1, C1, R2, and C2 simultaneously.



### Figure 30. Layout Example

## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Moisture Sensitivity and Soldering

Clear plastic does not contain the structural-enhancing fillers used in black plastic molding compound. As a result, clear plastic is more sensitive to environmental stress than black plastic. This can cause difficulties if devices have been stored in high humidity prior to soldering. The rapid heating during soldering can stress wire bonds and cause failures. Prior to soldering, it is recommended that plastic devices be baked-out at 85°C for 24 hours.

The fire-retardant fillers used in black plastic are not compatible with clear molding compound. The OPT101 plastic packages cannot meet flammability test, UL-94.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number     | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|---------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">OPT101P</a>   | Active        | Production           | PDIP (NTC)   8 | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | OPT101              |
| <a href="#">OPT101P-J</a> | Active        | Production           | SOP (DTL)   8  | 50   TUBE             | Yes         | NIPDAU                               | Level-4-250C-72 HR                | 0 to 70      | OPT101              |
| OPT101P-J.A               | Active        | Production           | SOP (DTL)   8  | 50   TUBE             | Yes         | NIPDAU                               | Level-4-250C-72 HR                | 0 to 70      | OPT101              |
| OPT101P.A                 | Active        | Production           | PDIP (NTC)   8 | 50   TUBE             | Yes         | NIPDAU                               | N/A for Pkg Type                  | 0 to 70      | OPT101              |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

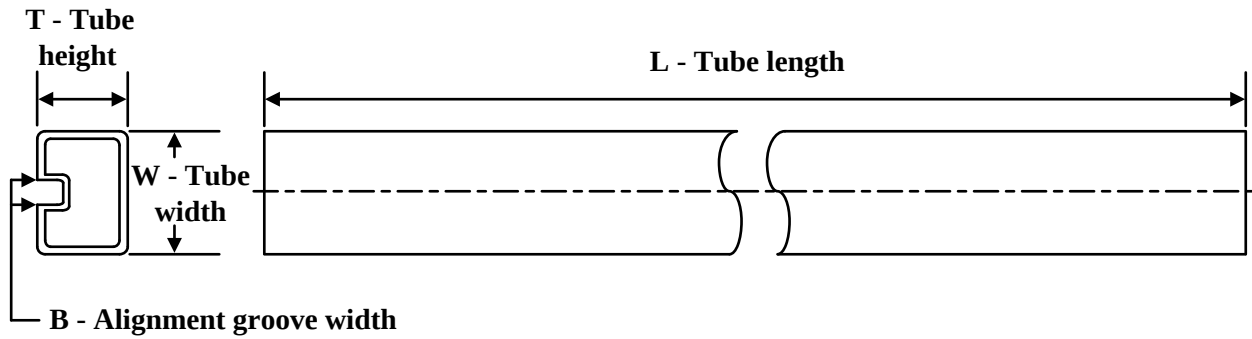
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

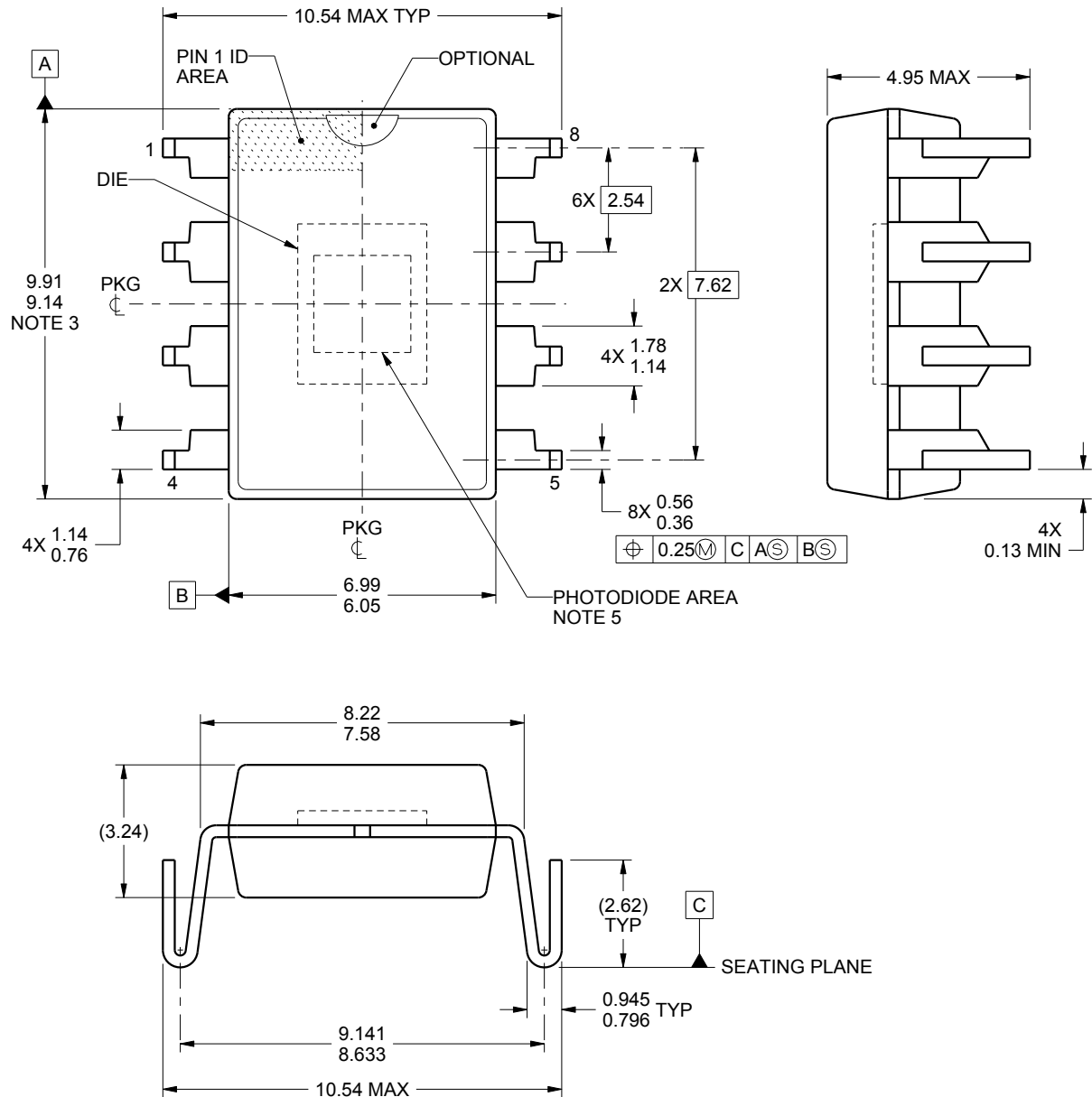
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TUBE



\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|-------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| OPT101P     | NTC          | PDIP         | 8    | 50  | 509    | 15.24  | 12.32  | 4.57   |
| OPT101P-J   | DTL          | SOP          | 8    | 50  | 530.5  | 14.8   | 7.7    | 5.5    |
| OPT101P-J.A | DTL          | SOP          | 8    | 50  | 530.5  | 14.8   | 7.7    | 5.5    |
| OPT101P.A   | NTC          | PDIP         | 8    | 50  | 509    | 15.24  | 12.32  | 4.57   |



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NOTES:

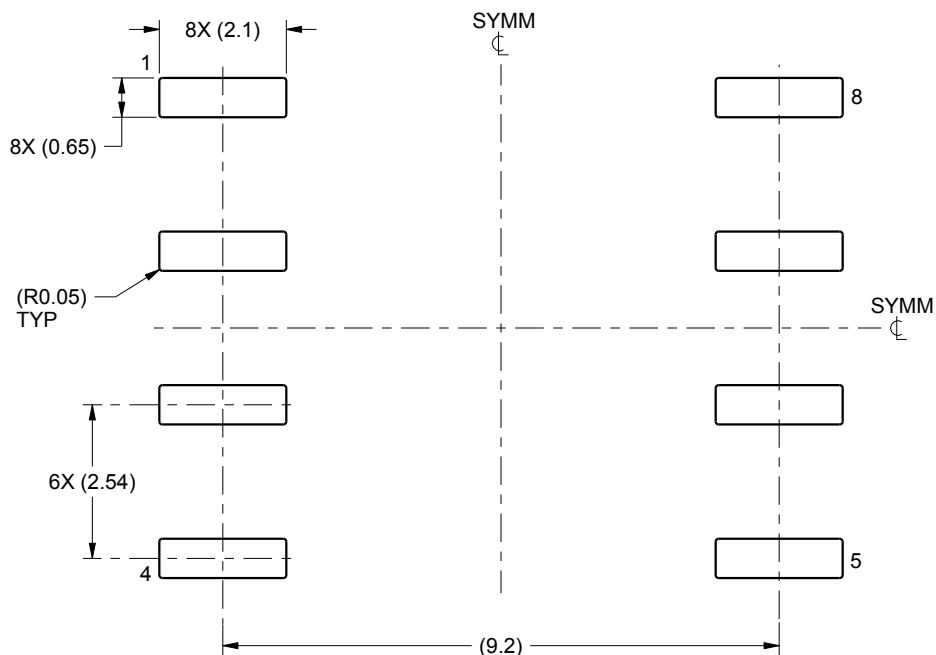
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
4. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.
5. Center of the photodiode must be within 0.25 of the center of the photodiode area.
6. The mold compound for this package is clear.

# EXAMPLE BOARD LAYOUT

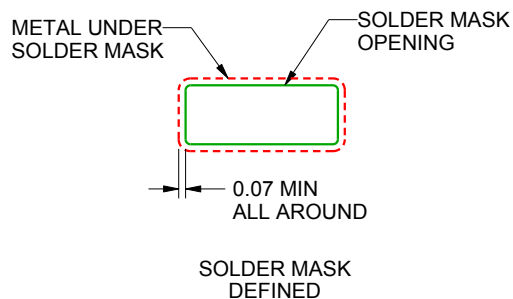
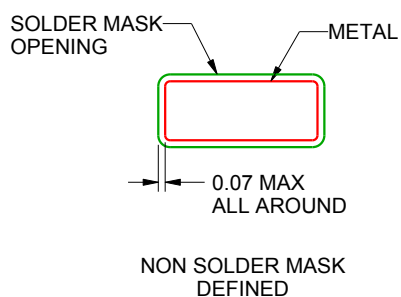
DTL0008A

SOP - 4.95 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:8X



SOLDER MASK DETAILS

4220739/B 02/2016

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.

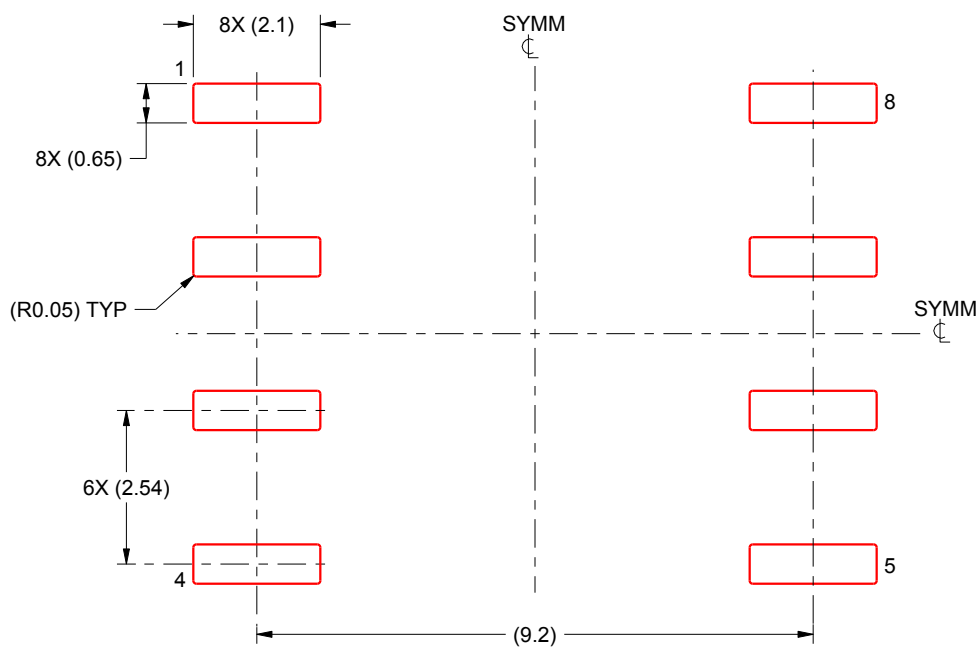
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DTL0008A

SOP - 4.95 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:8X

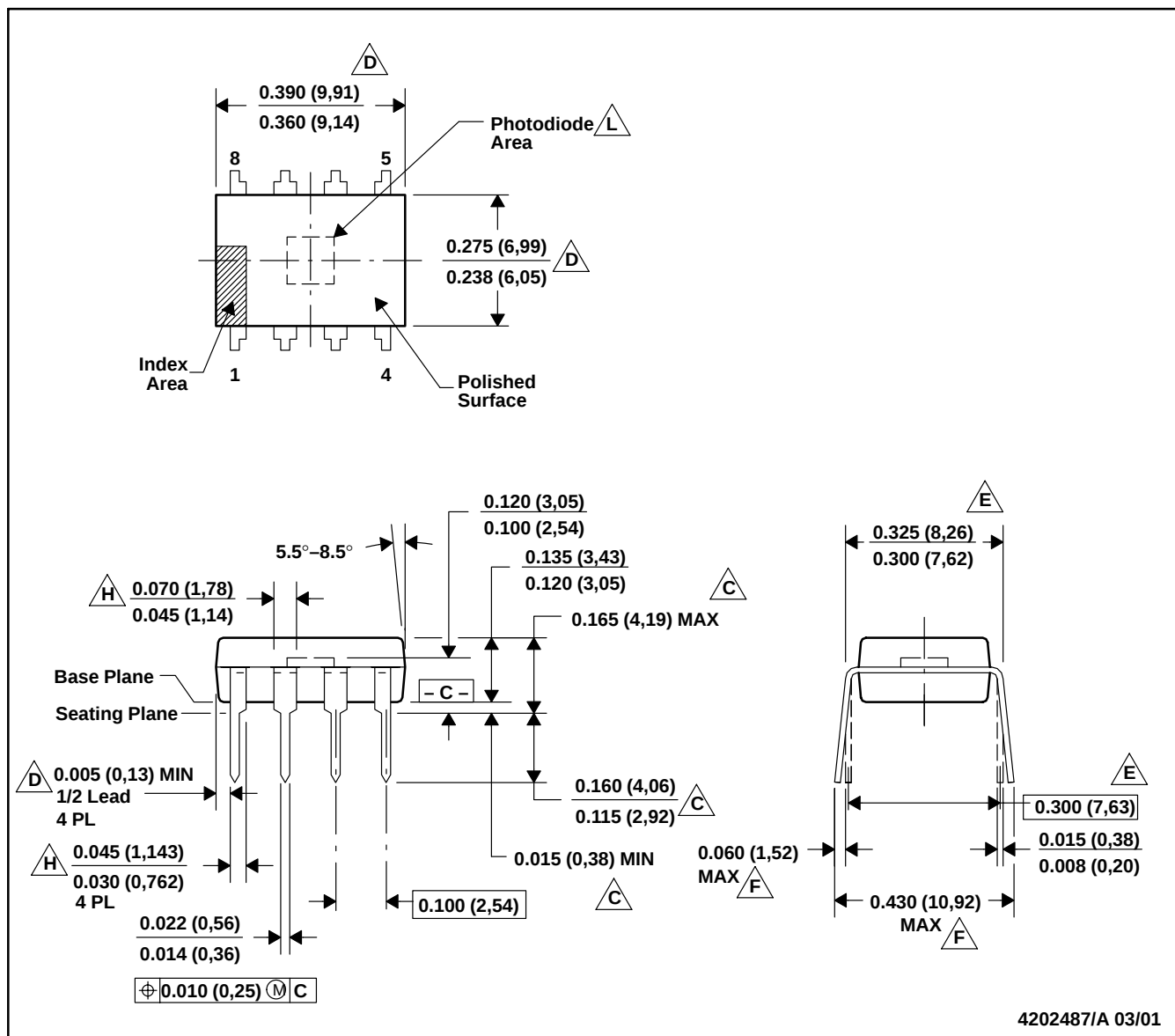
4220739/B 02/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

## NTC (R-PDIP-T8)

## PLASTIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C. Dimensions are measured with the package seated in JEDEC seating plane gauge GS-3.

D. Dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 (0,25).

E. Dimensions measured with the leads constrained to be perpendicular to Datum C.

F. Dimensions are measured at the lead tips with the leads unconstrained.

G. Pointed or rounded lead tips are preferred to ease insertion.

H. Maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0,25).

I. Distance between leads including dambar protrusions to be 0.005 (0,13) minimum.

J. A visual index feature must be located within the cross-hatched area.

K. For automatic insertion, any raised irregularity on the top surface (step, mesa, etc.) shall be symmetrical about the lateral and longitudinal package centerlines.

L. Center of photodiode must be within 0.010 (0,25) of center of photodiode area

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Last updated 10/2025